CLAIMS

1. A method of forming a capacitor electrode, comprising:

providing a sacrificial material sidewall at least partially around an opening;

forming a first silicon-containing material within the opening to partially fill the opening, the first silicon-containing material being doped with conductivity-enhancing dopant;

depositing a second silicon-containing material within the partially-filled opening; the second silicon-containing material being less heavily doped with conductivity-enhancing dopant than is the first silicon-containing material;

after depositing the second silicon-containing material, increasing a roughness of at least a portion of a surface thereof; and

removing at least some of the sacrificial material sidewall.

2. The method of claim 1 wherein the first silicon-containing material comprises a dopant concentration of at least 10^{20} atoms/cm^3.

3. The method of claim 1 wherein the first silicon-containing material comprises a dopant concentration that is at least 10^3 fold higher than any dopant concentration in the second silicon-containing material.

4. The method of claim 1 wherein the first silicon-containing material comprises a dopant concentration that is at least 10^5 fold higher than any dopant concentration in the second silicon-containing material.

5. The method of claim 1 wherein the first silicon-containing material comprises a dopant concentration that is at least 10^{10} fold higher than any dopant concentration in the second silicon-containing material.

6. The method of claim 1 wherein the second silicon-containing material is substantially undoped.

7. The method of claim 1 wherein the providing the sacrificial material sidewall at least partially around the opening comprises:

forming an insulative mass over a substrate;

forming the opening in the insulative mass; and

partially filling the opening with the sacrificial material.

8. A method of forming a capacitor electrode, comprising:

providing a sacrificial material sidewall at least partially around an opening;

forming a first silicon-containing material within the opening to partially fill the opening, the first silicon-containing material being doped with conductivity-enhancing dopant;

forming a second silicon-containing material within the partially-filled opening; the second silicon-containing material being less heavily doped with conductivity-enhancing dopant than is the first silicon-containing material;

converting at least some of a surface of the second silicon-containing material into a rugged silicon surface; and

removing at least some of the sacrificial material sidewall.

9. The method of claim 8 wherein the first silicon-containing material comprises a dopant concentration of at least 10^{20} atoms/cm^3.

10. The method of claim 8 wherein the first silicon-containing material comprises a dopant concentration that is at least 10^3 fold higher than any dopant concentration in the second silicon-containing material.

11. The method of claim 8 wherein the first silicon-containing material comprises a dopant concentration that is at least 10^5 fold higher than any dopant concentration in the second silicon-containing material.

12. The method of claim 8 wherein the first silicon-containing material comprises a dopant concentration that is at least 10^{10} fold higher than any dopant concentration in the second silicon-containing material.

13. The method of claim 8 wherein the second silicon-containing material is substantially undoped.

14. The method of claim 8 wherein the providing the sacrificial material sidewall at least partially around the opening comprises:

forming an insulative mass over a substrate;

forming the opening in the insulative mass; and

partially filling the opening with the sacrificial material.

15. The method of claim 8 wherein the sacrificial material is a metal-containing material; and wherein the providing the sacrificial material sidewall at least partially around the opening comprises:

forming an insulative mass over a substrate;

forming the opening in the insulative mass;

forming the sacrificial material within the opening and over an upper surface of the insulative mass; the sacrificial material partially filling the opening and being along sidewalls of the opening and along a bottom of the opening; and

exposing the sacrificial material to a plasma etch to remove the sacrificial material from over the upper surface of the mass and from along the bottom of the opening.

16. The method of claim 8 wherein the converting of at least some of the surface of the second silicon-containing material into a rugged silicon surface occurs before the removing at least some of the sacrificial material.

17. The method of claim 8 wherein the converting of at least some of the surface of the second silicon-containing material into a rugged silicon surface occurs after the removing of at least some of the sacrificial material; and wherein at least some of a surface of the first silicon-containing material is converted to a rugged silicon surface during the converting of at least some of the surface of the second silicon-containing material into a rugged silicon surface.

18. The method of claim 8 wherein,

the providing the sacrificial material sidewall at least partially around the opening comprises forming an insulative mass over a substrate; forming the opening in the insulative mass; and partially filling the opening with the sacrificial material;

the method further comprises forming the first and second silicon-containing materials over an upper surface of the insulative mass while forming the first and second silicon-containing materials in the opening;

the converting occurs while the first and second silicon-containing materials are over the upper surface of the insulative mass;

the first and second silicon-containing materials are removed from over the upper surface of the insulative mass after the converting;

at least some of the insulative mass is removed to expose a region of the sacrificial material sidewall; and

the removing of at least some of the sacrificial material sidewall comprises removing the exposed region of the sacrificial material sidewall.

19. The method of claim 18 wherein the exposed region of the sacrificial material sidewall is only a portion of the sacrificial material sidewall.

20. The method of claim 18 wherein the exposed region of the sacrificial material sidewall is an entirety of the sacrificial material sidewall.

21. The method of claim 8 wherein,

the providing the sacrificial material sidewall at least partially around the opening comprises forming an insulative mass over a substrate; forming the opening in the insulative mass; and partially filling the opening with the sacrificial material;

the method further comprises forming the first and second silicon-containing materials over an upper surface of the insulative mass while forming the first and second silicon-containing materials in the opening;

the first and second silicon-containing materials are removed from over the upper surface of the insulative mass, and at least some of the insulative mass is removed to expose a region of the sacrificial material sidewall; and

the removing of at least some of the sacrificial material sidewall comprises removing the exposed region of the sacrificial material sidewall.

22. The method of claim 21 wherein the converting occurs after the removing of the at least some of the sacrificial material sidewall.

23. The method of claim 21 wherein the converting occurs before the removing of the at least some of the sacrificial material sidewall.

24. The method of claim 21 wherein the exposed region of the sacrificial material sidewall is only a portion of the sacrificial material sidewall.

25. The method of claim 21 wherein the exposed region of the sacrificial material sidewall is an entirety of the sacrificial material sidewall.

26. A method of forming a semiconductor construction, comprising:

providing a substrate having an opening extending therein; the opening having a periphery defined by at least one sidewall and a bottom; the substrate having an upper surface proximate the opening;

forming a stack comprising layers of sacrificial material, first silicon-containing material and second silicon-containing material along the sidewall of the opening; the second silicon-containing material having a higher concentration of conductivity-enhancing dopant than the first silicon-containing material;

removing some of the substrate to lower the upper surface of the substrate and thereby expose at least a portion of the sacrificial material;

removing at least some of the exposed portion of the sacrificial material; and

converting the first silicon-containing material to hemispherical grain silicon.

27. The method of claim 26 wherein the first and second silicon-containing materials extend across the bottom of the opening, and wherein the sacrificial material does not extend across a majority of the bottom of the opening.

28. The method of claim 26 wherein the converting occurs before the removing of at least some of the exposed portion of the sacrificial material.

29. The method of claim 26 wherein the converting occurs after the removing of at least some of the exposed portion of the sacrificial material.

30. The method of claim 26 wherein the converting occurs after the removing at least some of the exposed portion of the sacrificial material and wherein the converting further comprises converting at least some of the second silicon-containing material to hemispherical grain silicon during the conversion of the at least some of the first silicon-containing material to hemispherical grain silicon.

31. The method of claim 26 wherein the converting occurs before the removing of some of the substrate.

32. The method of claim 26 wherein the converting occurs after the removing of some of the substrate.

33. The method of claim 26 wherein the converting occurs after the removing of some of the substrate and before the removing at least some of the exposed portion of the sacrificial material.

34. The method of claim 26 wherein the sacrificial material comprises a metal.

35. The method of claim 26 wherein the sacrificial material comprises elemental titanium.

36. The method of claim 26 wherein the sacrificial material comprises elemental tungsten.

37. The method of claim 26 wherein the sacrificial material comprises a metal nitride.

38. The method of claim 26 wherein the sacrificial material comprises titanium nitride.

39. The method of claim 26 wherein the sacrificial material comprises tungsten nitride.

40. The method of claim 26 wherein the substrate comprises borophosphosilicate glass, and wherein the opening is formed into the borophosphosilicate glass.

41. The method of claim 26 wherein the second silicon-containing material is substantially undoped.

42. A method of forming a capacitor structure, comprising:

forming a container construction comprising a first silicon-containing layer around a second silicon-containing layer; the first silicon-containing layer being more heavily doped with conductivity-enhancing dopant than the second silicon-containing layer; the second silicon-containing layer defining an inner periphery of the container and the first silicon-containing layer defining an outer periphery of the container;

converting at least some of each of the first and second silicon-containing layers to hemispherical grain silicon; the hemispherical grain silicon from the first silicon-containing layer having a smaller average grain size than the hemispherical grain silicon from the second silicon-containing layer;

forming a dielectric material along the inner and outer peripheries of the container construction; and

forming a conductive material over the dielectric material; the container construction, dielectric material and conductive material together defining at least part of the capacitor structure.

43. The method of claim 42 wherein the converting comprises:

(1) exposing the at least some of each of the first and second silicon-containing layers to silane gas and a temperature of at least about 550°C for a time of less than or equal to about 2 minutes under a vacuum of less than or equal to about 1×10^{-4} Torr to seed the at least some of each of the first and second silicon-containing layers; and

(2) annealing the seeded layers at a temperature of at least about 550°C for a time of less than or equal to about 3 minutes.

44. The method of claim 42 wherein the first silicon-containing layer comprises a dopant concentration of at least 10^{20} atoms/cm^3.

45. The method of claim 42 wherein the first silicon-containing layer comprises a dopant concentration that is at least 10^3 fold higher than any dopant concentration in the second silicon-containing layer.

46. The method of claim 42 wherein the first silicon-containing layer comprises a dopant concentration that is at least 10^5 fold higher than any dopant concentration in the second silicon-containing layer.

47. The method of claim 42 wherein the first silicon-containing layer comprises a dopant concentration that is at least 10^{10} fold higher than any dopant concentration in the second silicon-containing layer.

48. The method of claim 42 wherein the second silicon-containing layer is substantially undoped.

49. A method of forming a capacitor structure, comprising:

providing a substrate having an electrical node supported thereby;

forming an insulative mass over the electrical node;

forming an opening extending through the insulative mass to the electrical node; the opening having a periphery which includes at least one sidewall;

forming a first layer along the at least one sidewall of the opening;

forming a second layer along first layer; the second layer comprising silicon which is doped with a conductivity-enhancing dopant;

forming a third layer along the second layer; any concentration of conductivity-enhancing dopant in the third layer being less than the concentration of conductivity-enhancing dopant in the second layer;

removing some of the insulative mass to expose at least a portion of the first layer;

removing at least some of the exposed portion of the first layer to expose at least some of the second layer;

converting at least some of the third layer to hemispherical grain silicon;

forming a dielectric material along the third layer and exposed portion of the second layer; and

forming a conductive material over the dielectric material; the second layer, third layer, dielectric material and conductive material together defining at least part of the capacitor structure.

50. The method of claim 49 wherein the first layer comprises a metal.

51. The method of claim 49 wherein the second layer comprises a dopant concentration of at least 10^{20} atoms/cm^3.

52. The method of claim 49 wherein the second layer comprises a dopant concentration that is at least 10^3 fold higher than any dopant concentration in the third layer.

53. The method of claim 49 wherein the second layer comprises a dopant concentration that is at least 10^5 fold higher than any dopant concentration in the third layer.

54. The method of claim 49 wherein the second layer comprises a dopant concentration that is at least 10^{10} fold higher than any dopant concentration in the third layer.

55. The method of claim 49 wherein the converting occurs before the removing at least some of the exposed portion of the first layer.

56. The method of claim 49 wherein the converting occurs after the removing at least some of the exposed portion of the first layer.

57. The method of claim 49 wherein the converting occurs after the removing at least some of the exposed portion of the first layer and wherein the converting further comprises converting at least some of the second layer to hemispherical grain silicon during the conversion of the at least some of the third layer to hemispherical grain silicon.

58. The method of claim 49 wherein the converting occurs before the removing of some of the insulative mass.

59. The method of claim 49 wherein the converting occurs after the removing of some of the insulative mass.

60. The method of claim 49 wherein the converting occurs after the removing of some of the insulative mass and before the removing at least some of the exposed portion of the first layer.

61. A capacitor structure comprising:

a container construction comprising a first silicon-containing layer around a second silicon-containing layer; the second silicon-containing layer defining an inner periphery of the container construction and the first silicon-containing layer defining an outer periphery of the container construction; the outer periphery of the container construction having a smoother surface than the inner periphery of the container construction;

at least some of the second silicon-containing layer being in the form of hemispherical grain silicon;

a dielectric material along the inner and outer peripheries of the container construction; and

a conductive material over the dielectric material; the container construction, dielectric material and conductive material together defining at least part of the capacitor structure.

62. The capacitor structure of claim 61 wherein the first silicon-containing layer is more heavily doped with conductivity-enhancing dopant than the second silicon-containing layer.

63. The capacitor structure of claim 61 wherein at least some of the first silicon-containing layer is in the form of hemispherical grain silicon; the hemispherical grain silicon of the first silicon-containing layer having a smaller average grain size than the hemispherical grain silicon of the second silicon-containing layer.

64. A capacitor-containing assembly, comprising:

a substrate supporting an electrical node;

an insulative mass over the substrate and having an opening extending therethrough to the electrical node; the opening having a sidewall periphery and a bottom periphery; the insulative mass having an upper surface proximate the opening;

a conductive material extending along the sidewall periphery of the opening, but not extending along a majority of the bottom periphery of the opening; the conductive material not extending above the upper surface of the insulative mass;

a first silicon-containing layer against the conductive material and within the opening; the first silicon-containing layer defining a container shape extending along the sidewall periphery of the opening and along the bottom periphery of the opening; the first silicon-containing layer extending to above the upper surface of the insulative mass; an outer surface of the container shape of the first silicon-containing layer having a first roughness;

a second silicon-containing layer within the container-shape defined by the first silicon-containing layer; the second silicon-containing layer extending along the sidewall periphery of the opening and along the bottom periphery of the opening; the second silicon-containing layer extending to above the upper surface of the insulative mass;

at least some of the second silicon-containing layer being in the form of a rugged silicon having a surface roughness greater than the first roughness;

a dielectric material against the second silicon-containing layer and against a portion the first silicon-containing layer; and

a conductive material over the dielectric material; the container first and second silicon-containing layers, dielectric material and conductive material together defining at least part of the capacitor structure.

65. The assembly of claim 64 wherein the insulative mass comprises borophosphosilicate glass.

66. The assembly of claim 64 wherein the conductive material comprises a metal.

67. The assembly of claim 64 wherein the conductive material comprises elemental titanium.

68. The assembly of claim 64 wherein the conductive material comprises elemental tungsten.

69. The assembly of claim 64 wherein the conductive material comprises a metal nitride.

70. The assembly of claim 64 wherein the conductive material comprises titanium nitride.

71. The assembly of claim 64 wherein the conductive material comprises tungsten nitride.

72. The assembly of claim 64 wherein the first silicon-containing layer is more heavily doped with conductivity-enhancing dopant than the second silicon-containing layer.

73. The assembly of claim 64 wherein at least some of the first silicon-containing layer of the outer surface is in the form of hemispherical grain silicon and wherein the rugged silicon of the second silicon-containing layer is in the form of hemispherical grain silicon; the hemispherical grain silicon of the first silicon-containing layer having a smaller average grain size than the hemispherical grain silicon of the second silicon-containing layer.